Semi Design Presents..

CMOS Fabrication Process
[p-well method]

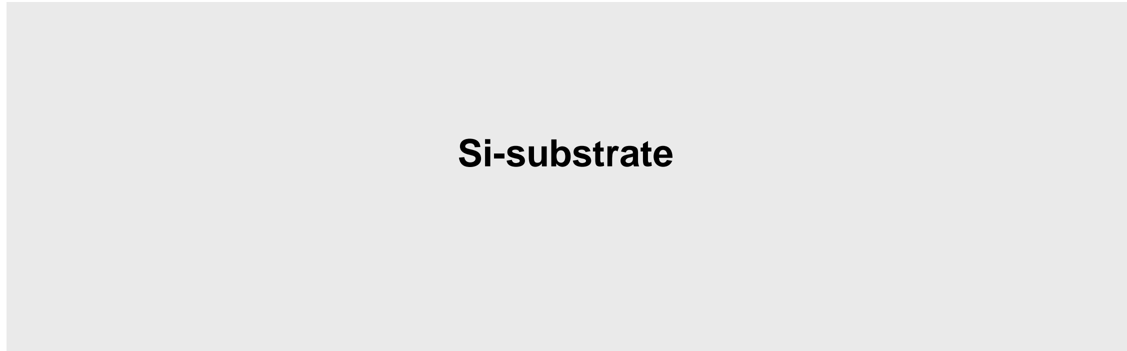


Fig. (1) Pure Si single crystal

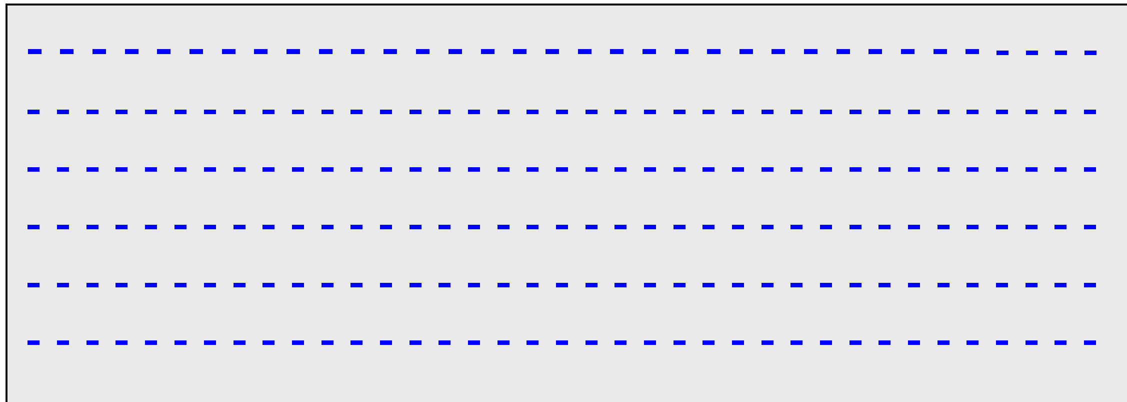


Fig. (2) n-type impurity is lightly doped

N-MOS Fabrication Process
[Step- formation of p-well]

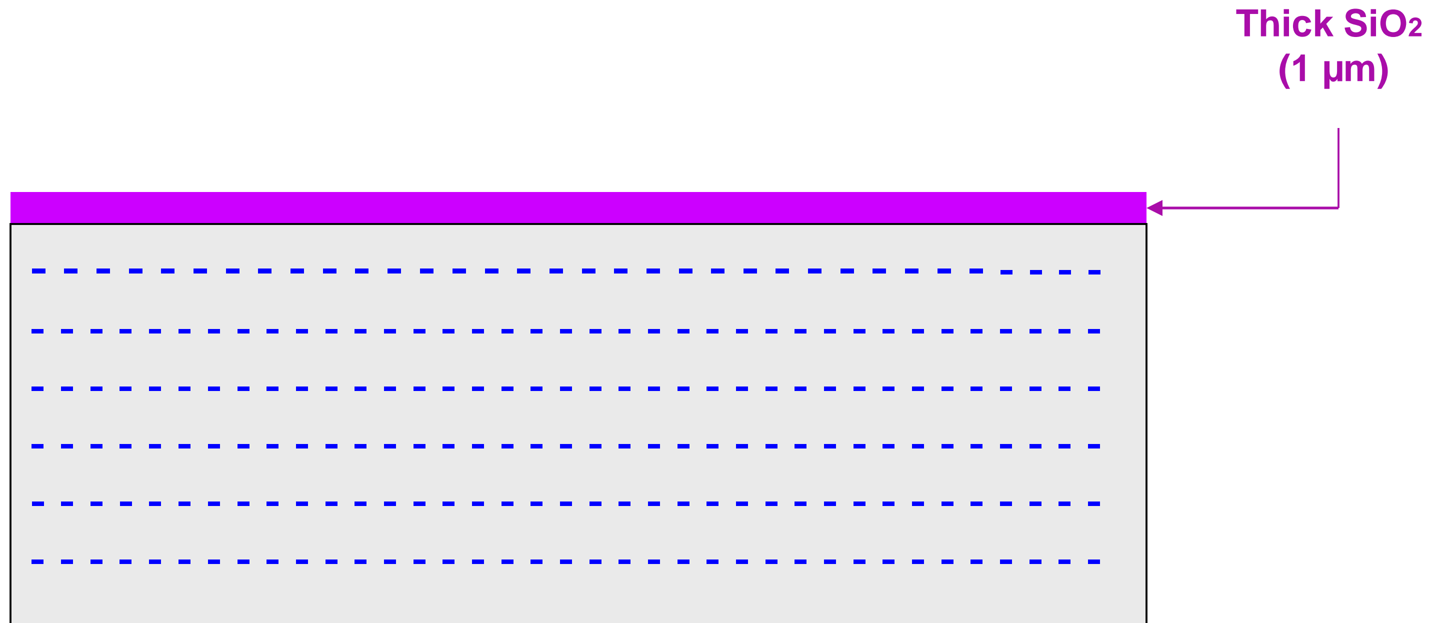


Fig. (3) SiO_2 Deposited over si surface

N-MOS Fabrication Process
[Step- formation of p-well]

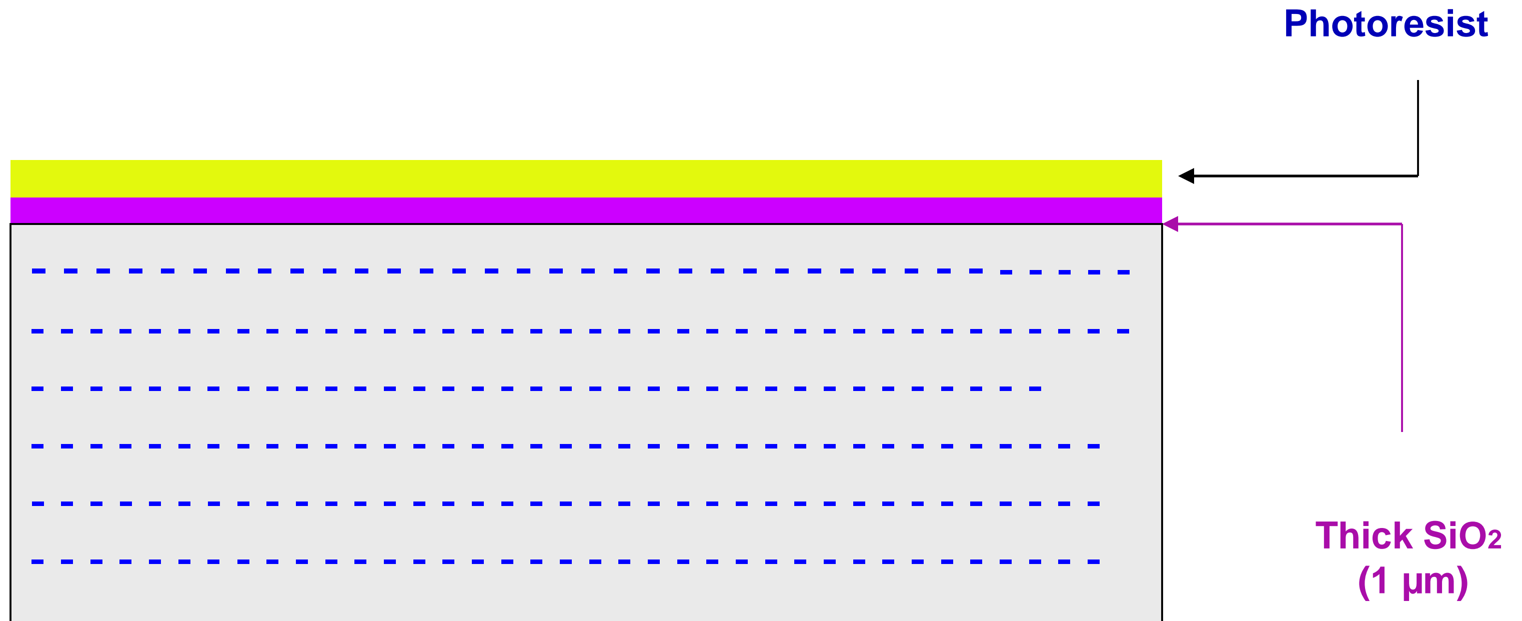


Fig. (4) Photoresist is Deposited over siO_2 surface

N-MOS Fabrication Process
[Step- formation of p-well]

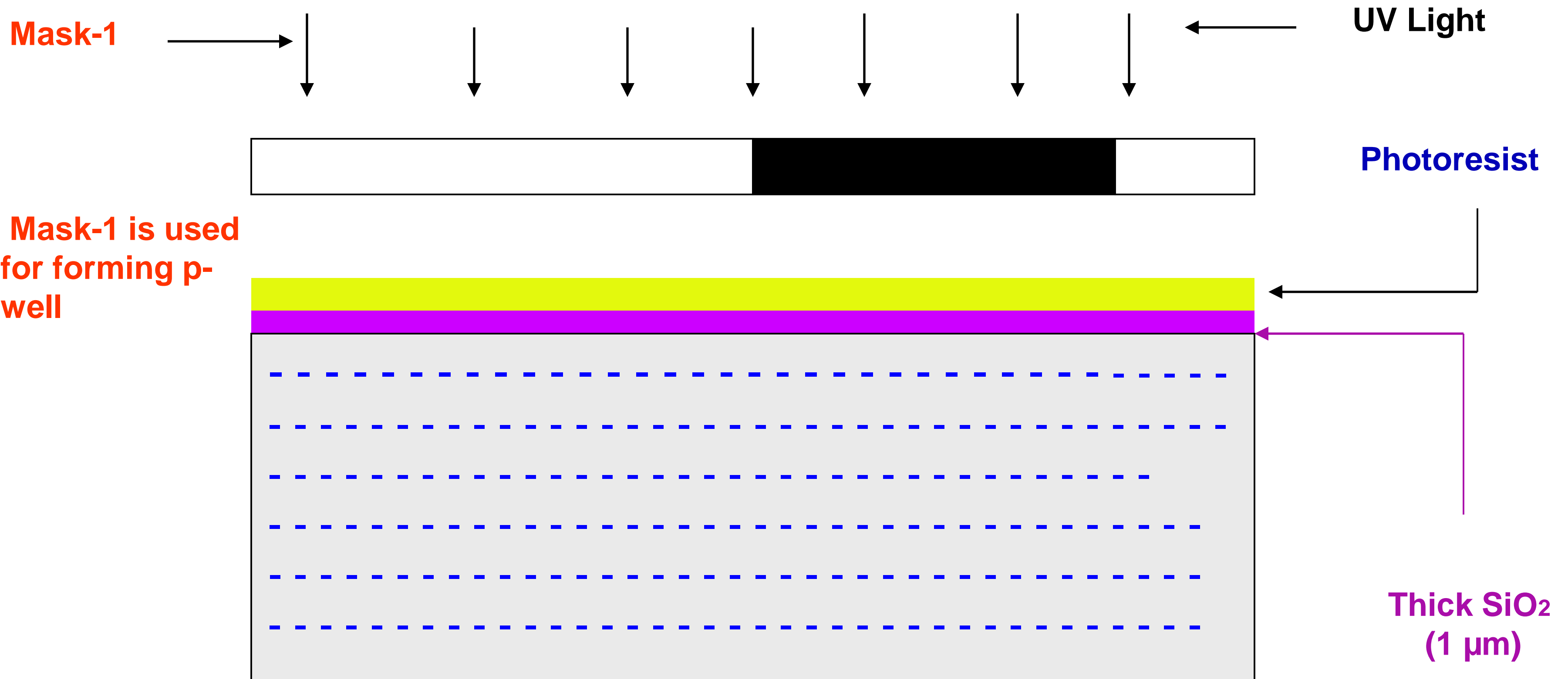


Fig. (5) Photoresist is Deposited over siO_2 surface

N-MOS Fabrication Process [Step- formation of p-well]

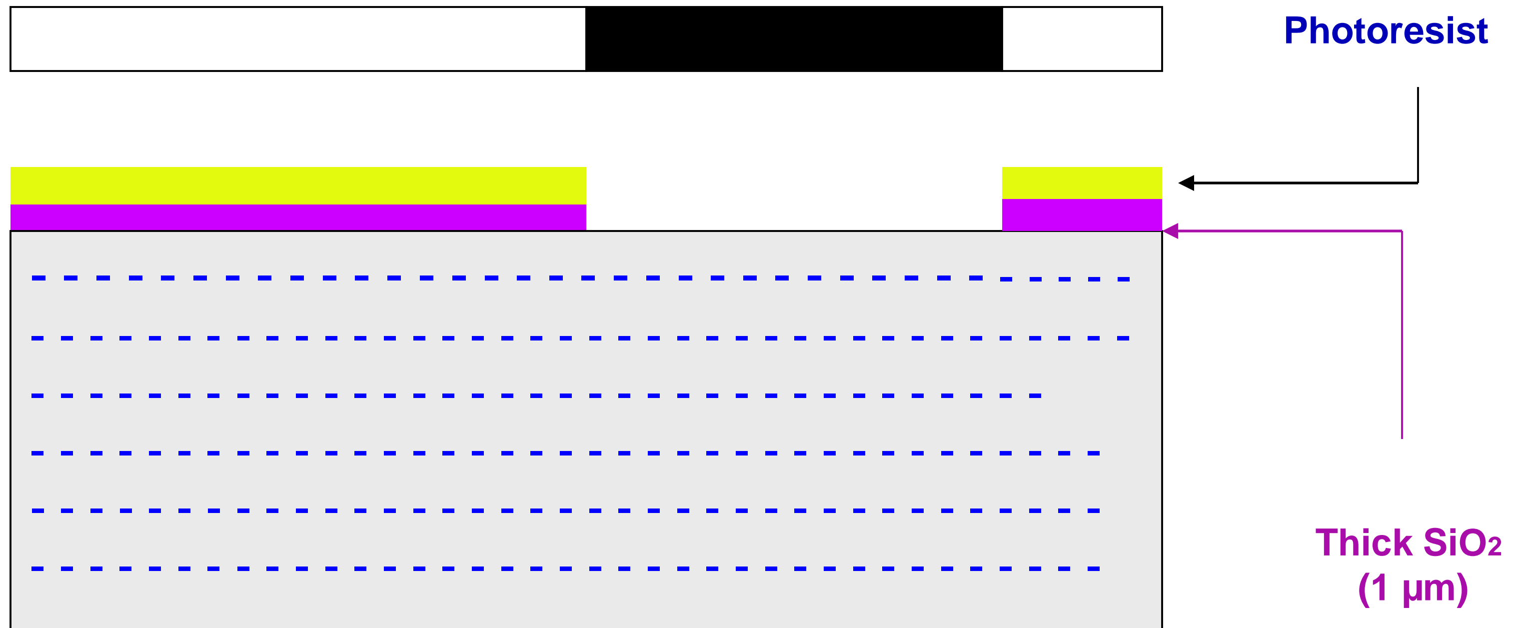


Fig. (6) Photoresist and SiO2 which is not exposed is etched away.

N-MOS Fabrication Process
[Step- formation of p-well]

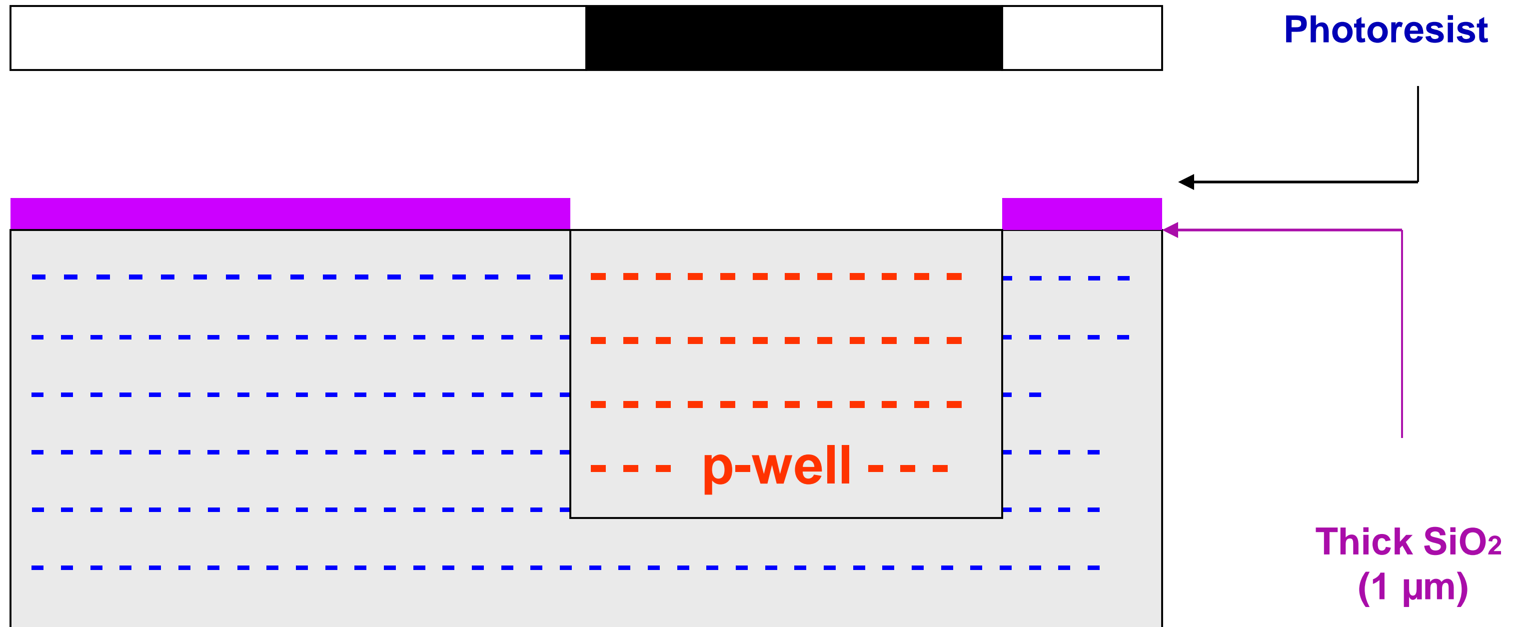


Fig. (7) Hardened Photoresist is stripped away and p-type impurity is added by diffusion process.

N-MOS Fabrication Process
[Step- formation of Diffusion area for p-MOS]

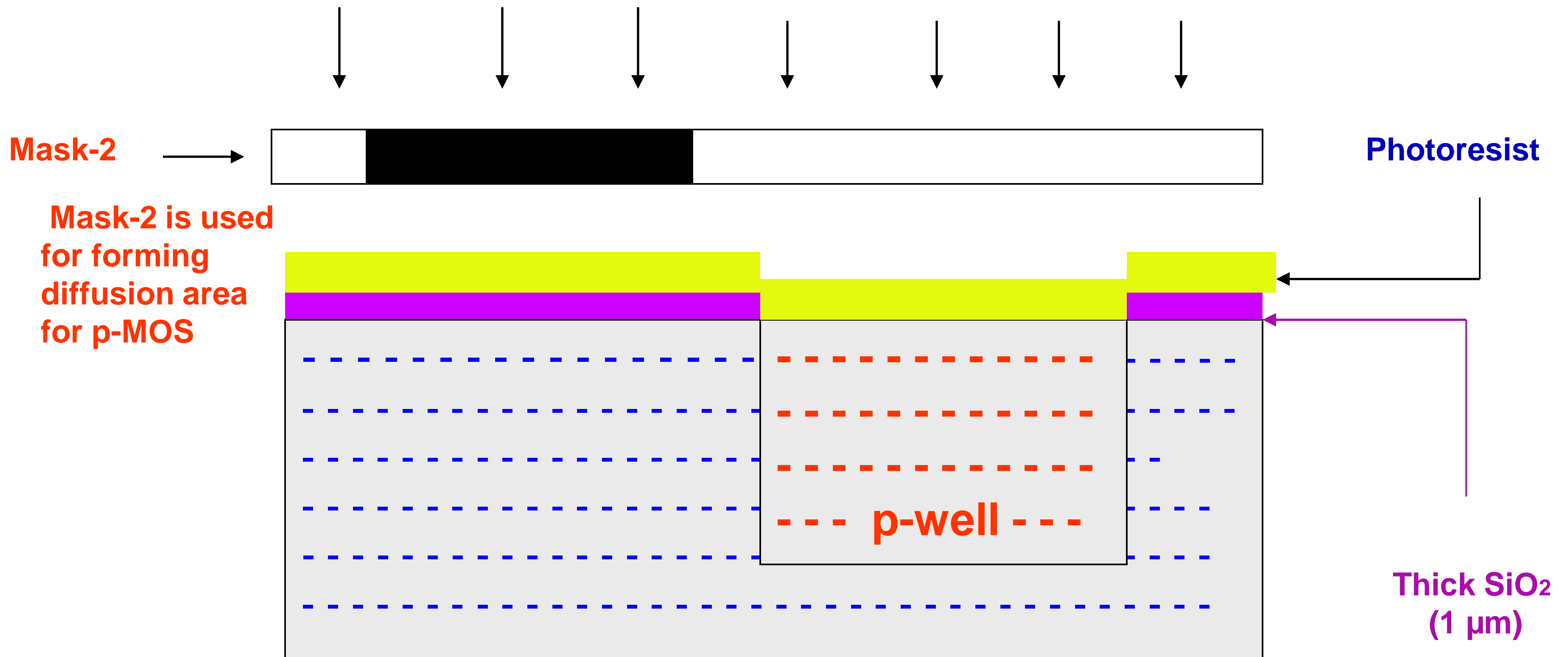


Fig. (8) Photo resist is grown and exposed in UV Light.

N-MOS Fabrication Process
[Step- formation of Diffusion area for p-MOS]

Fig. (9) Photoresist and SiO_2 which are un-exposed are etched away.

N-MOS Fabrication Process
[Step- formation of Diffusion area for p-MOS]

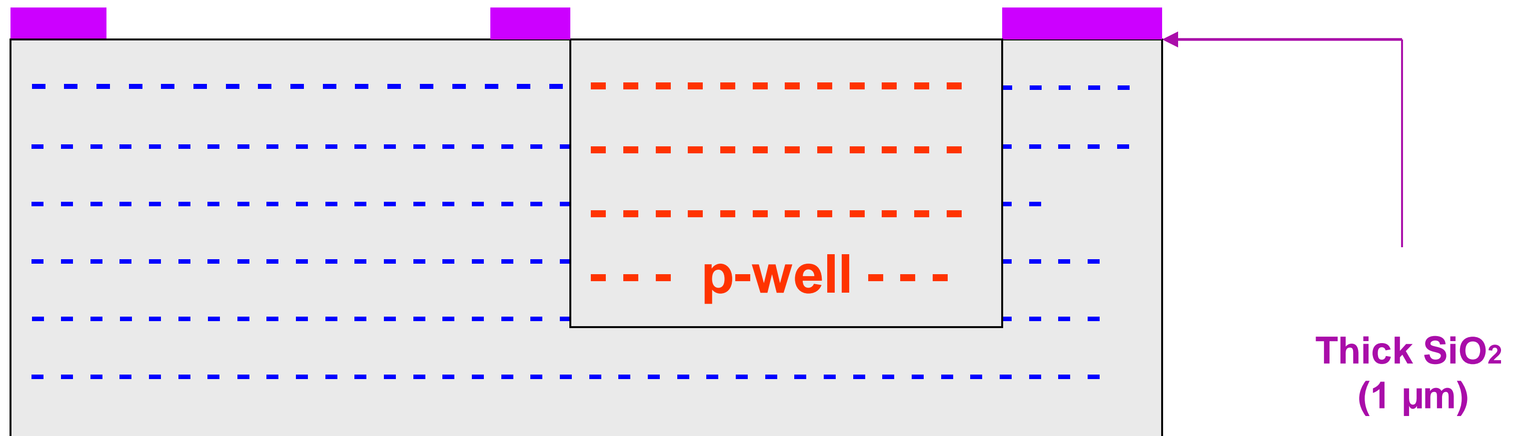


Fig. (10) Polymerised Photoresist is stripped away.

N-MOS Fabrication Process

[[Step- Gate formation for n-MOS and p-MOS]

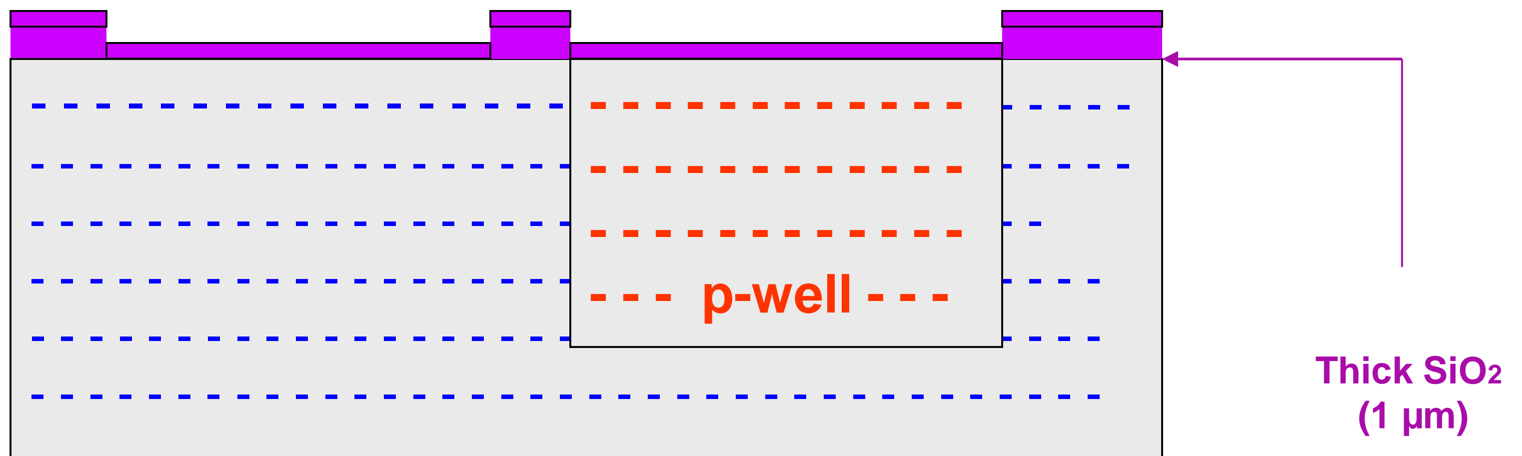


Fig. (11) Deposit Thinox

N-MOS Fabrication Process

[[Step- Gate formation for n-MOS and p-MOS]

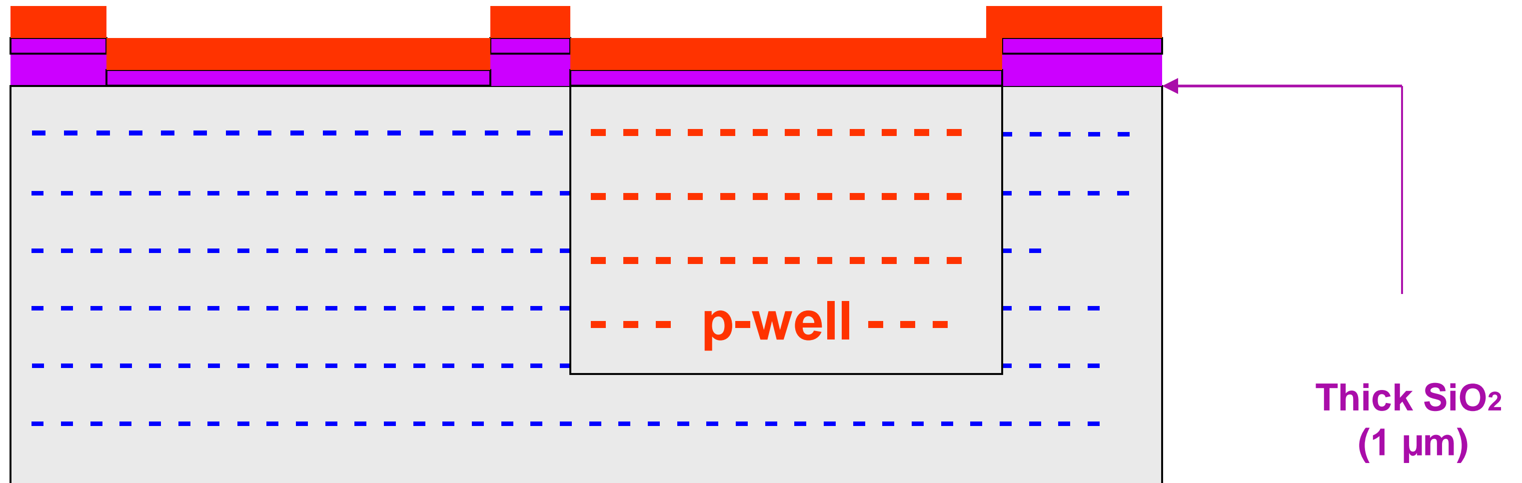


Fig. (12) Deposit Polysilicon

N-MOS Fabrication Process

[[Step- Gate formation for n-MOS and p-MOS]

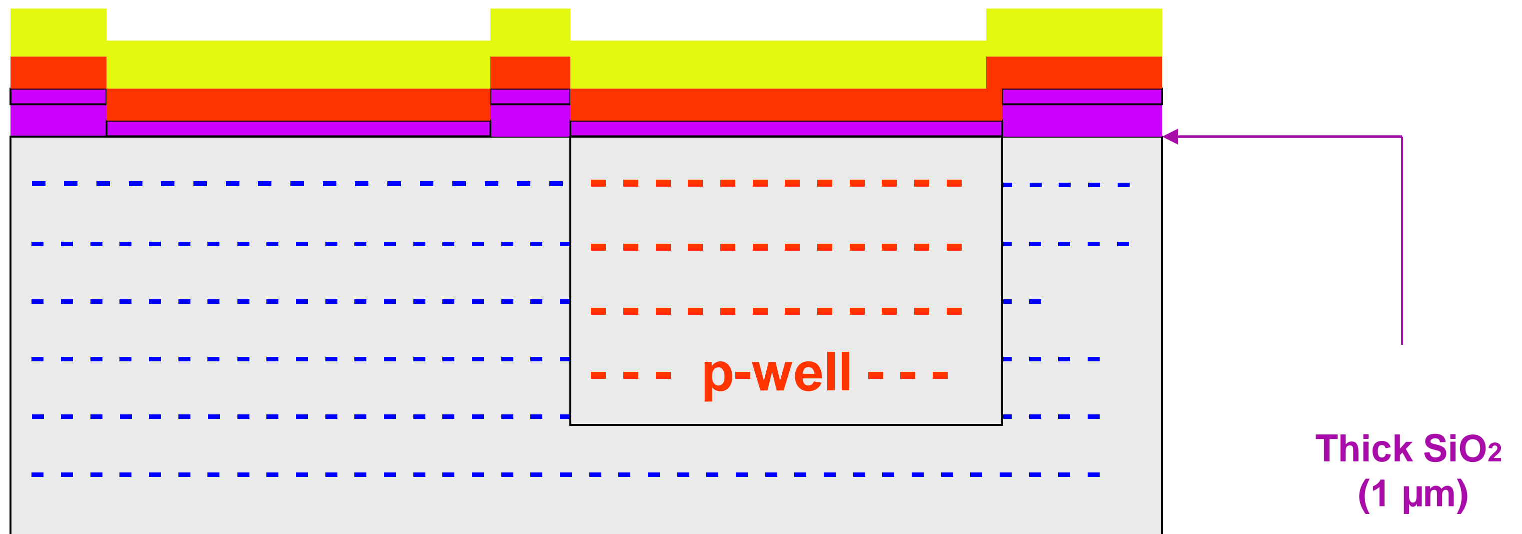


Fig. (13) Deposit Photoresist

N-MOS Fabrication Process

[[Step- Gate formation for n-MOS and p-MOS]

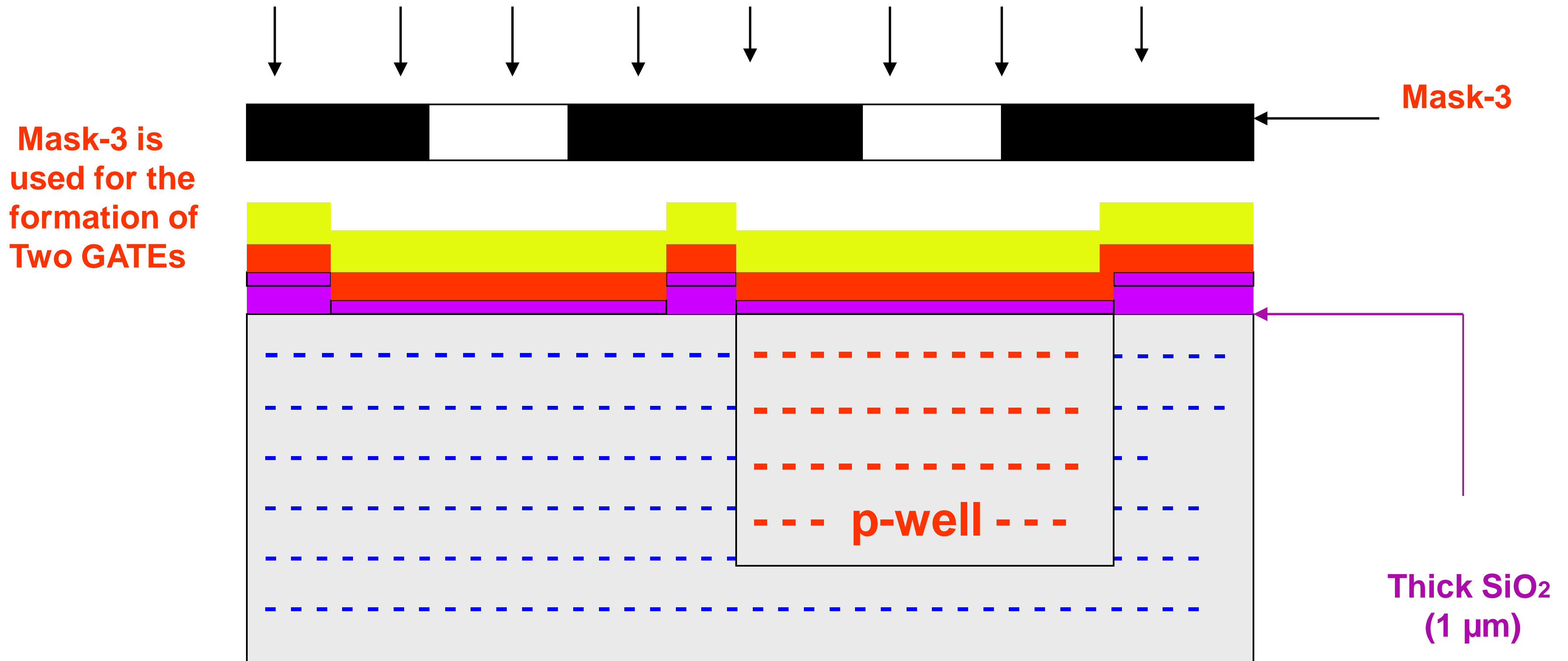


Fig. (14) UV Light Exposure to form GATEs of P-MOS and n-MOS

N-MOS Fabrication Process

[[Step- Gate formation for n-MOS and p-MOS]

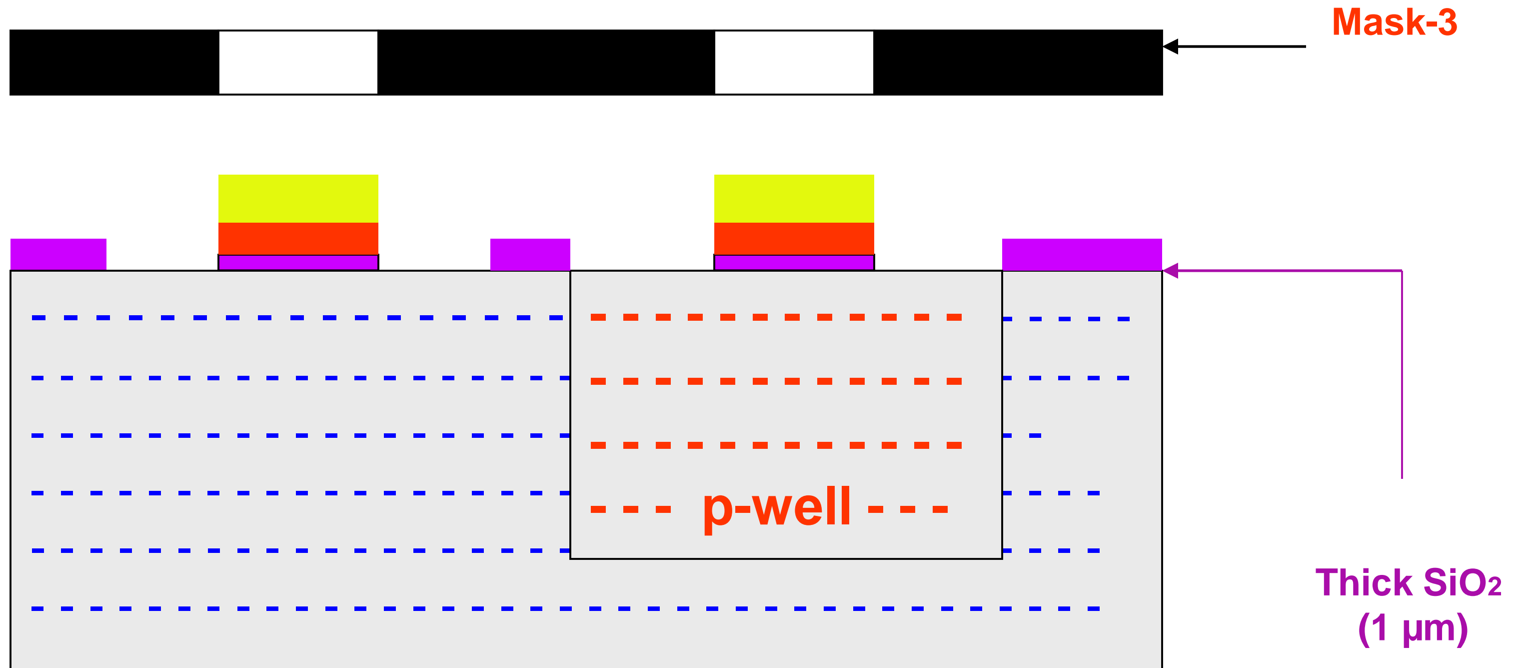


Fig. (15) Un-Exposed Photoresist, Metal and Thinox is etched away.

N-MOS Fabrication Process

[[Step- Gate formation for n-MOS and p-MOS]

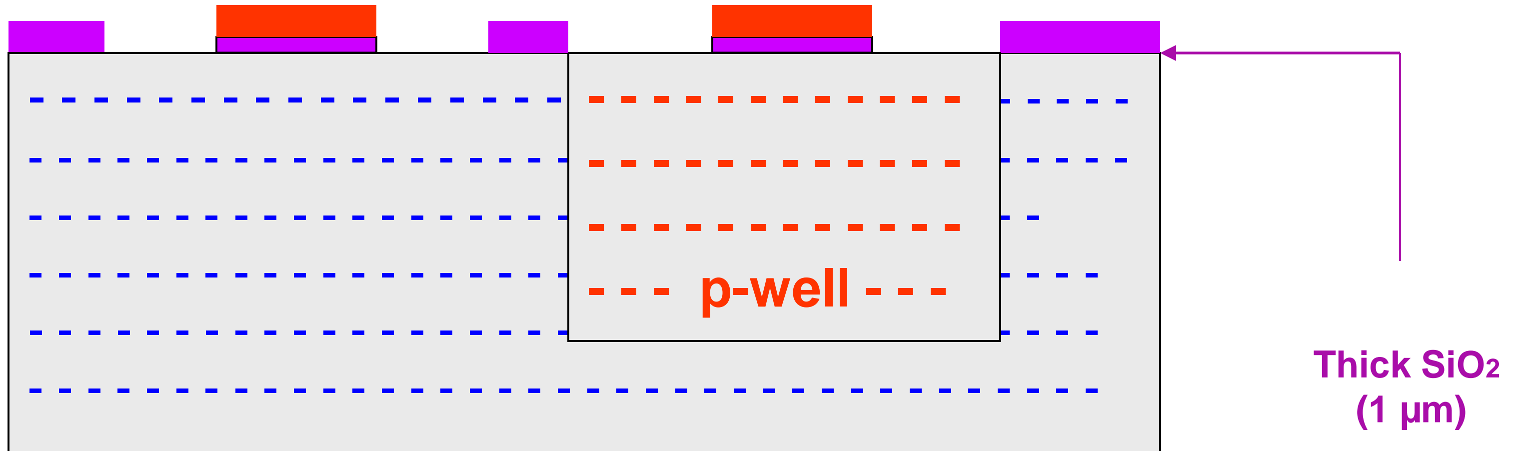


Fig. (16) Polymerised Photoresist is stripped away.

N-MOS Fabrication Process

[[Step- Source & Drain formation for p-MOS]

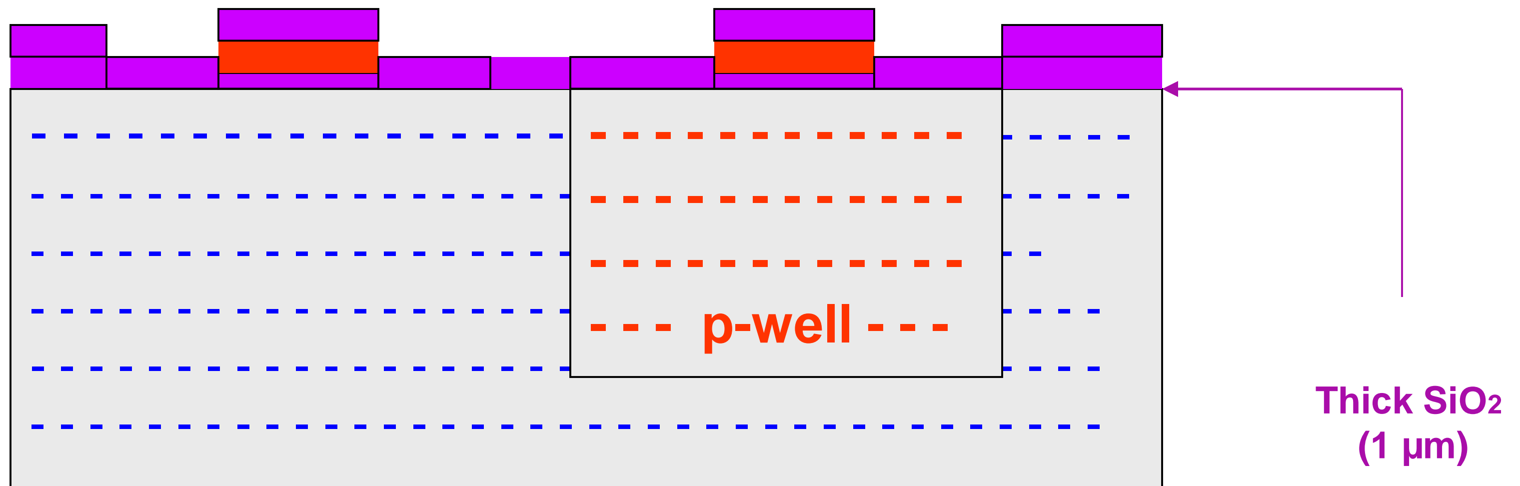


Fig. (17) Grow SiO_2 Layer

N-MOS Fabrication Process

[[Step- Source & Drain formation for p-MOS]

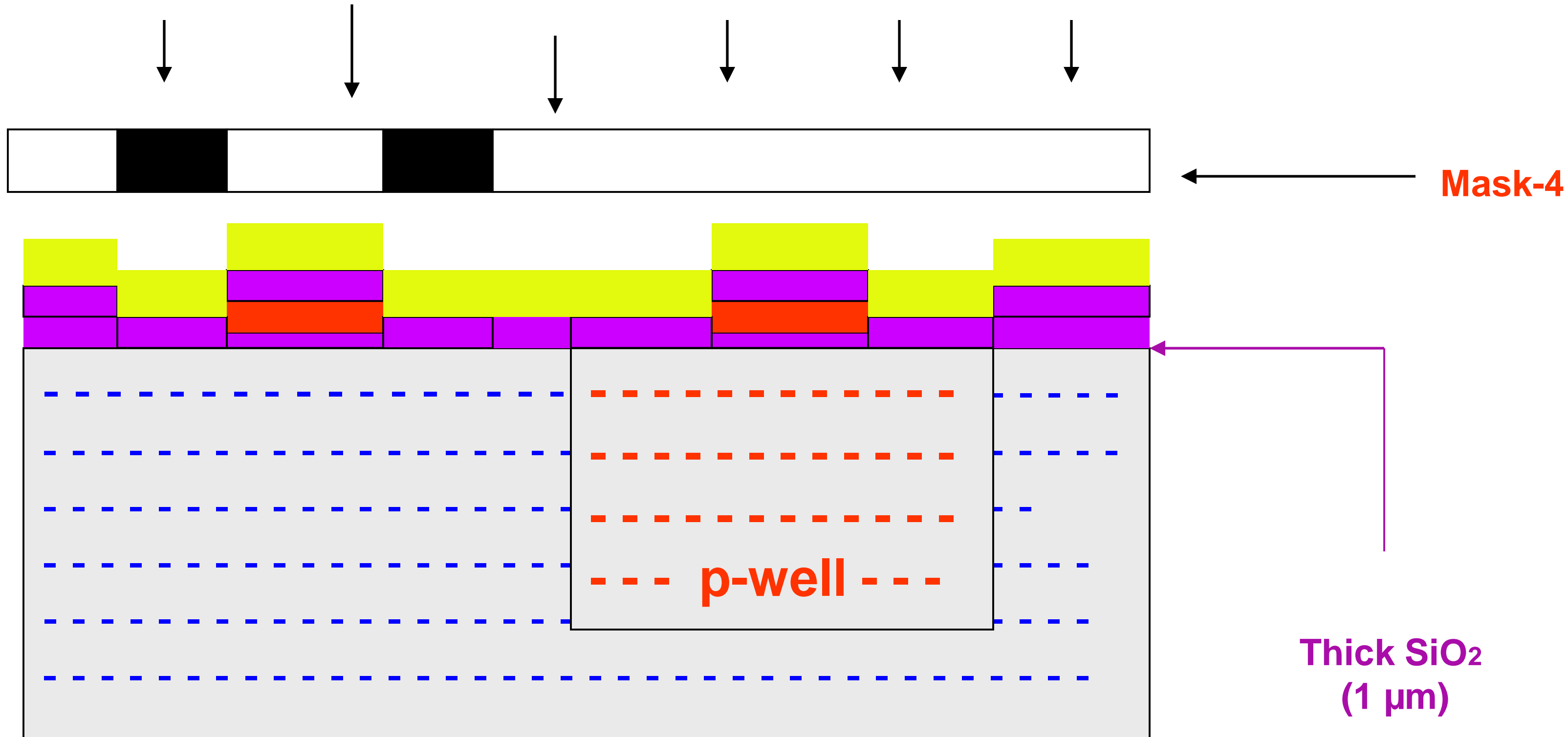


Fig. (18) Grow Photoresist Layer

N-MOS Fabrication Process

[[Step- Source & Drain formation for p-MOS]

Mask-4 is used for the formation of S and D of p-MOS

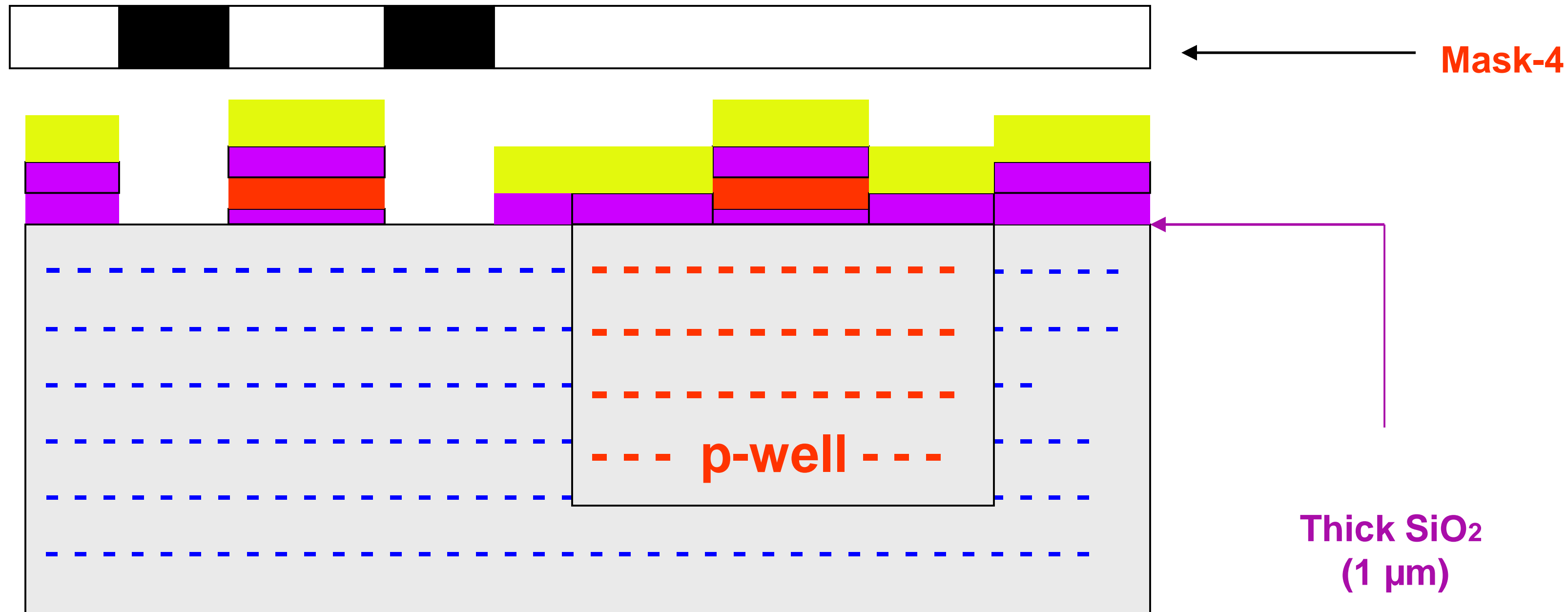


Fig. (19) Etching of un[polymerised photoresist and SiO_2 below it

N-MOS Fabrication Process

[[Step- Source & Drain formation for p-MOS]

Mask-4 is used for the formation of S and D of p-MOS

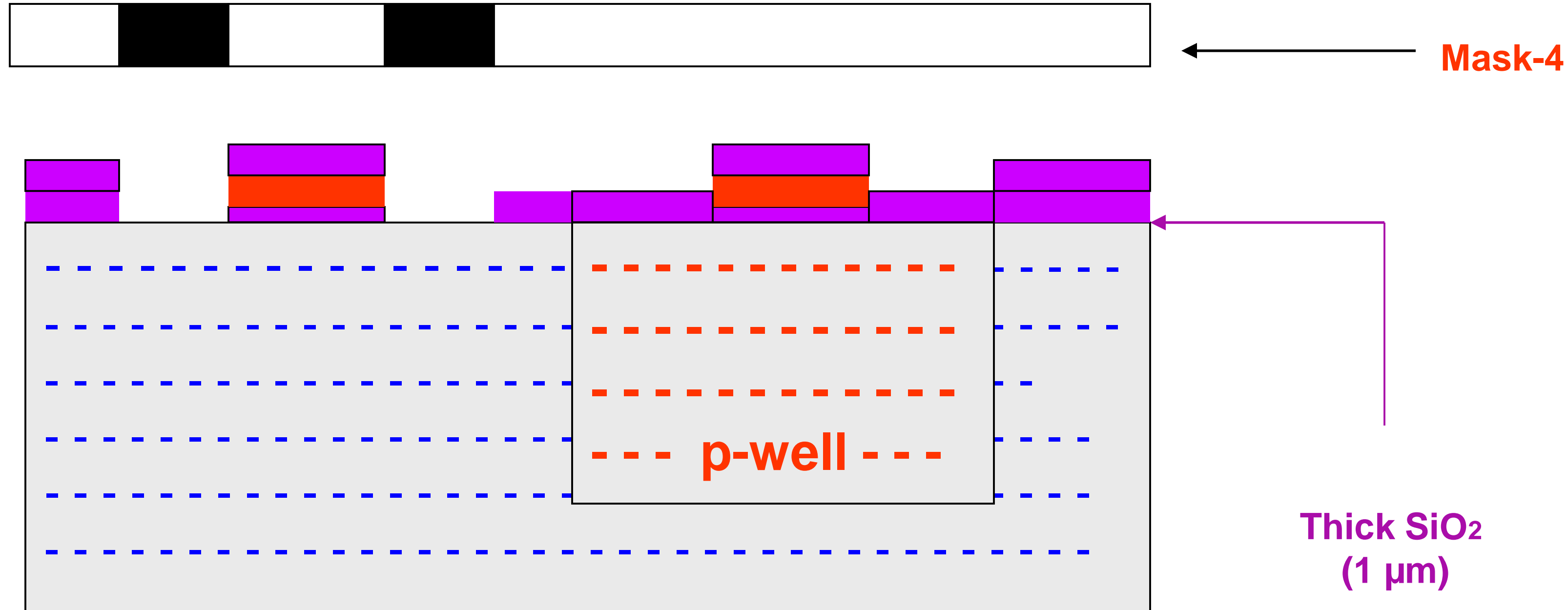


Fig. (20) Strip away hard photoresist

N-MOS Fabrication Process

[[Step- Source & Drain formation for p-MOS]

Mask-4 is used for the formation of S and D of p-MOS

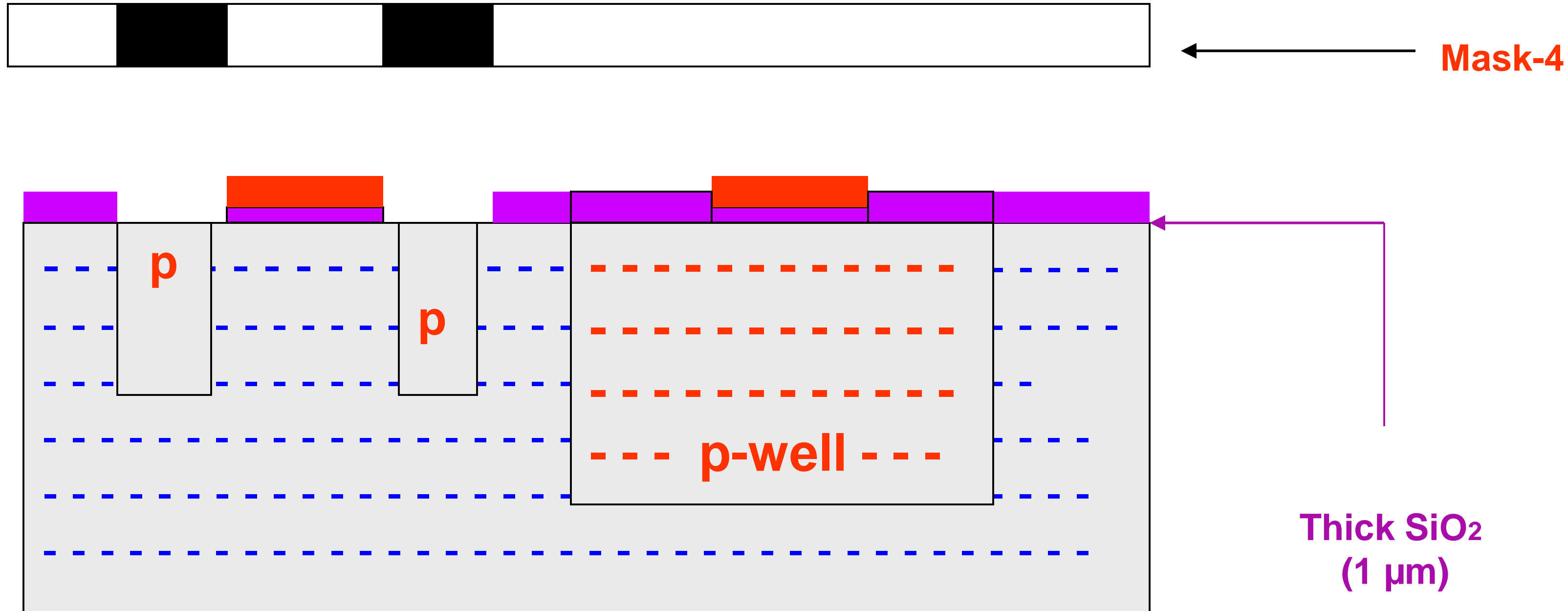


Fig. (21) Diffusion of p-type impurity

N-MOS Fabrication Process

[[Step- Source & Drain formation for n-MOS]

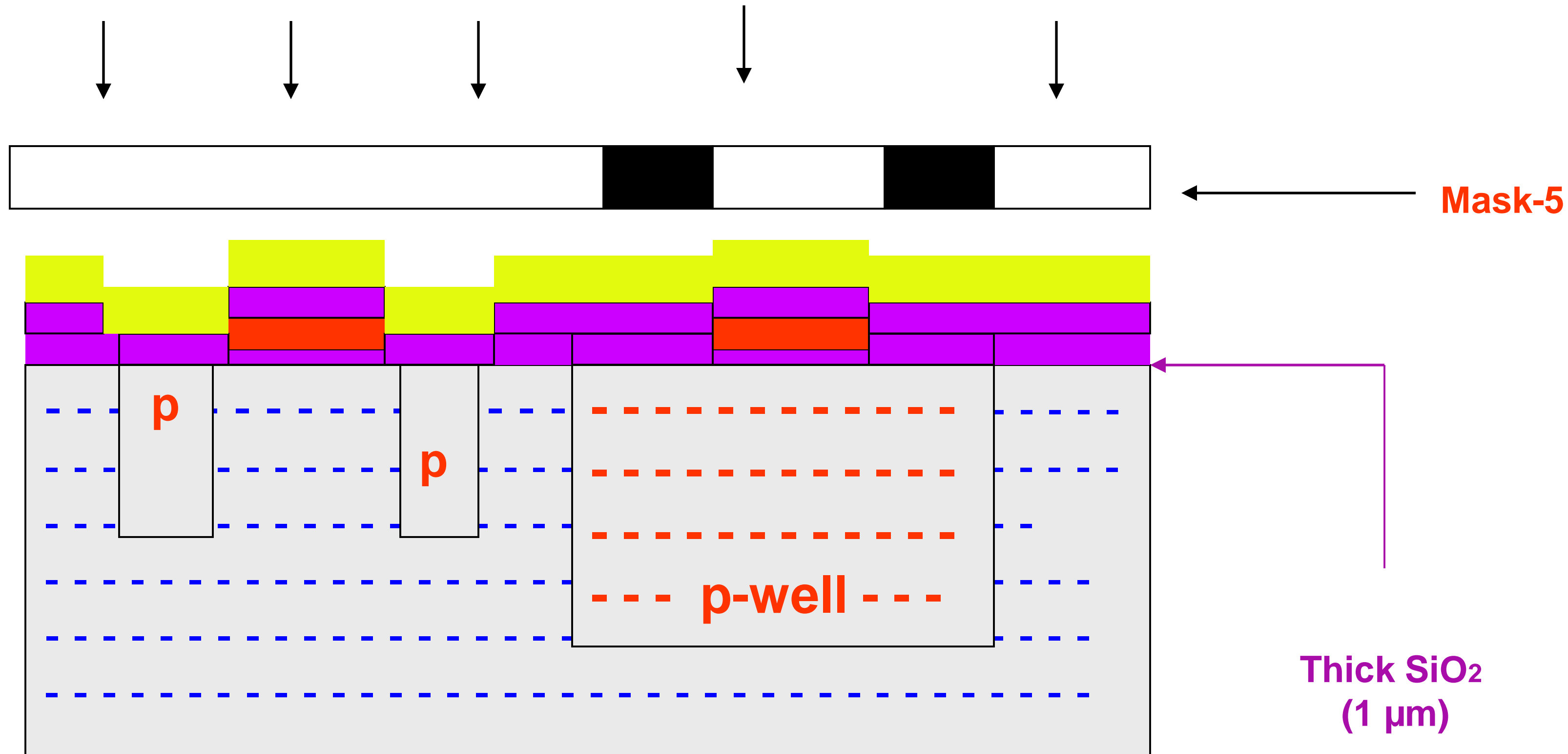


Fig. (22) Grow photoresist

N-MOS Fabrication Process

[[Step- Source & Drain formation for n-MOS]

Mask-5 is used for the formation of S and D of n-MOS

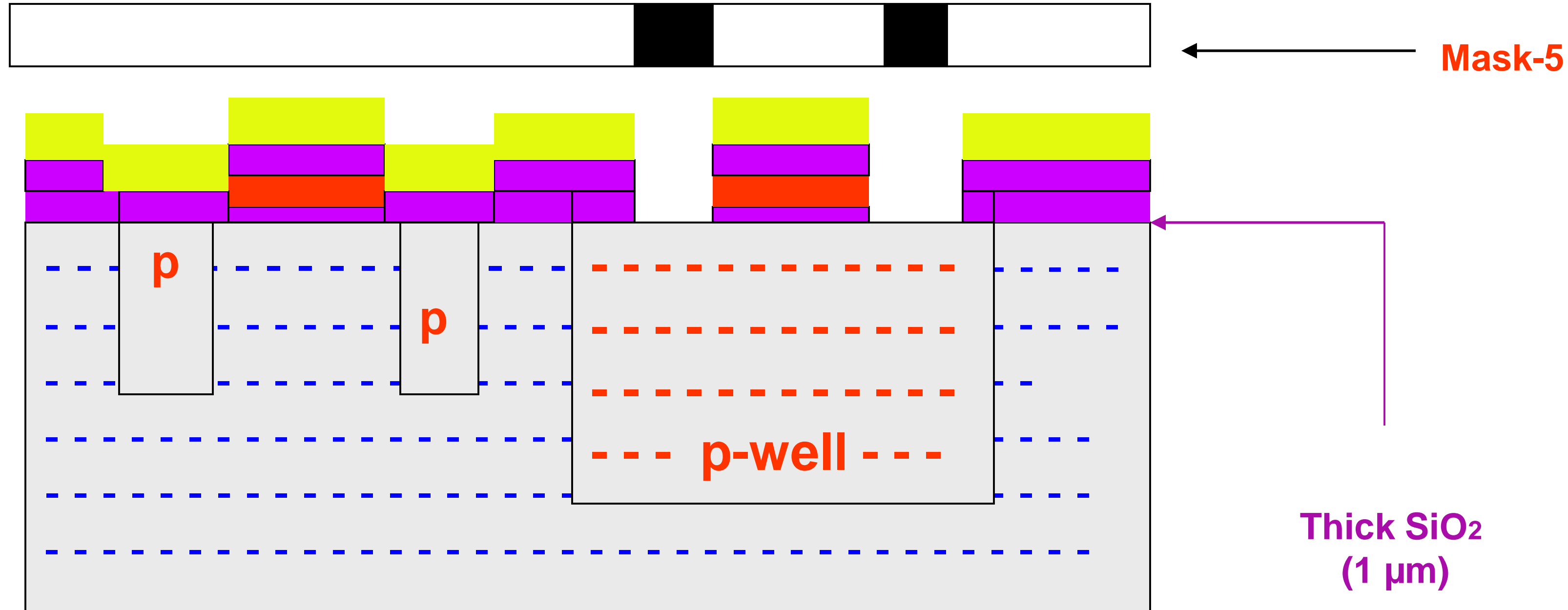


Fig. (23) Etching

N-MOS Fabrication Process

[[Step- Source & Drain formation for n-MOS]

Mask-5 is used for the formation of S and D of n-MOS

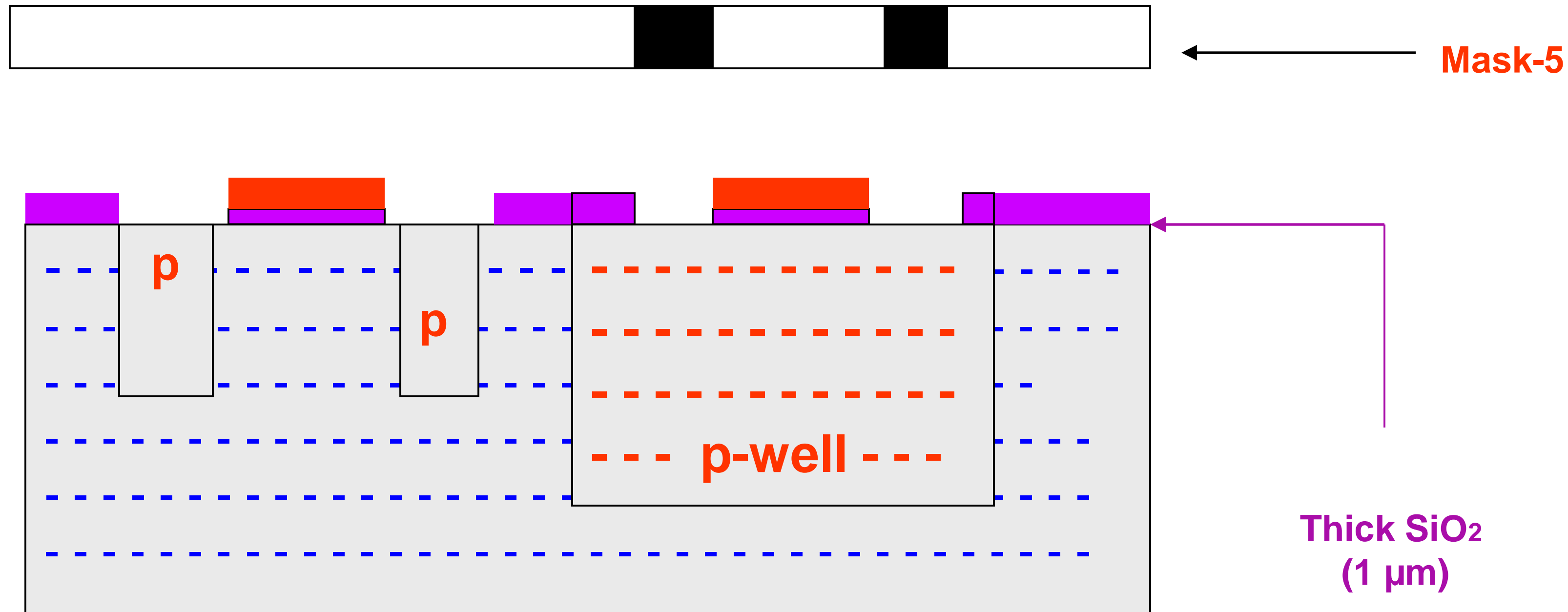


Fig. (24) Hard photoresist stripped away

N-MOS Fabrication Process

[[Step- Source & Drain formation for n-MOS]

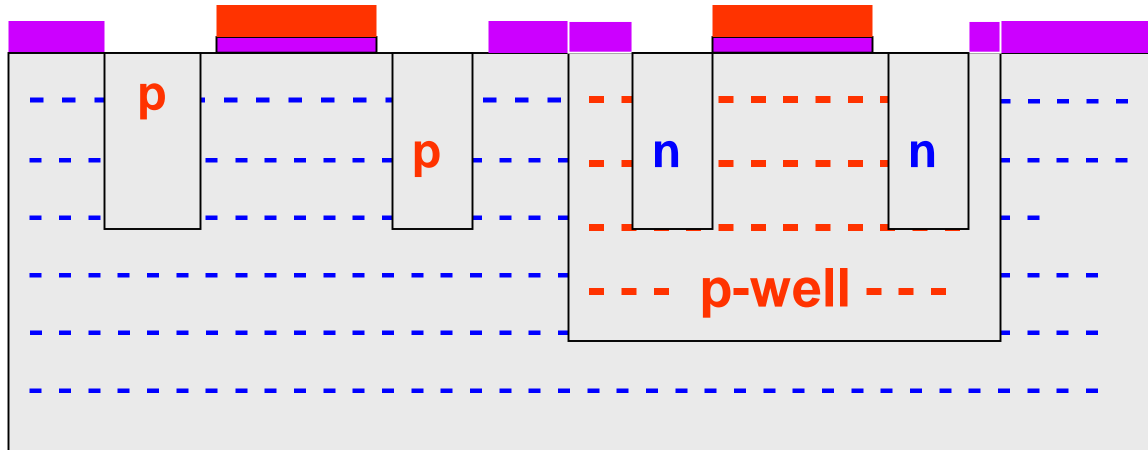
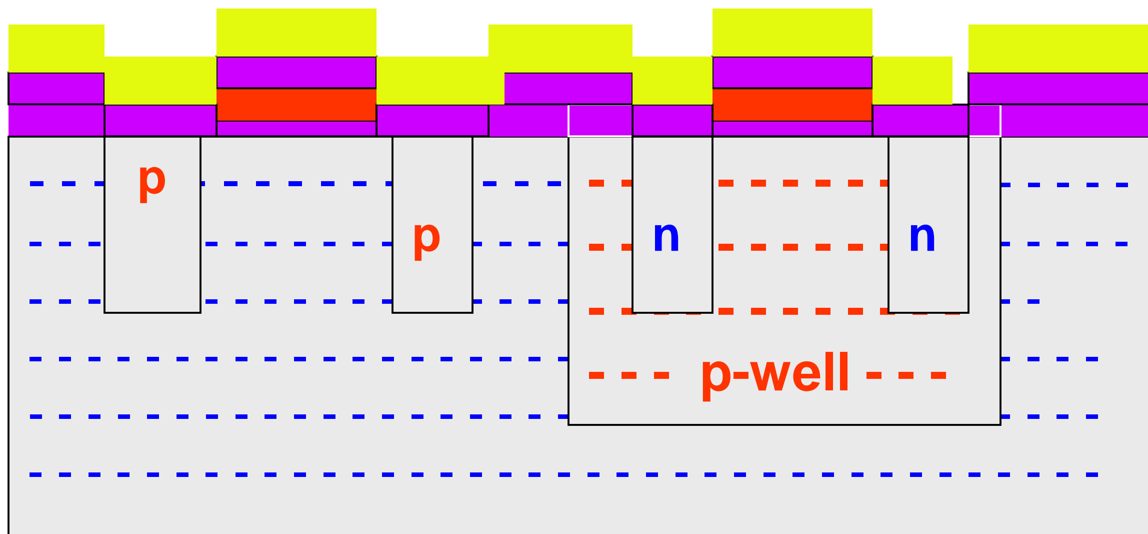


Fig. (25) Diffusion of n-type impurity to form Source and Drain of n-MOS

N-MOS Fabrication Process

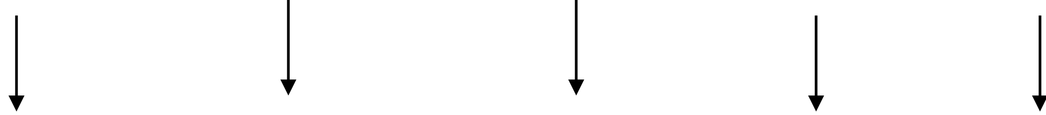
[[Step- Formation of Contact-Cut]

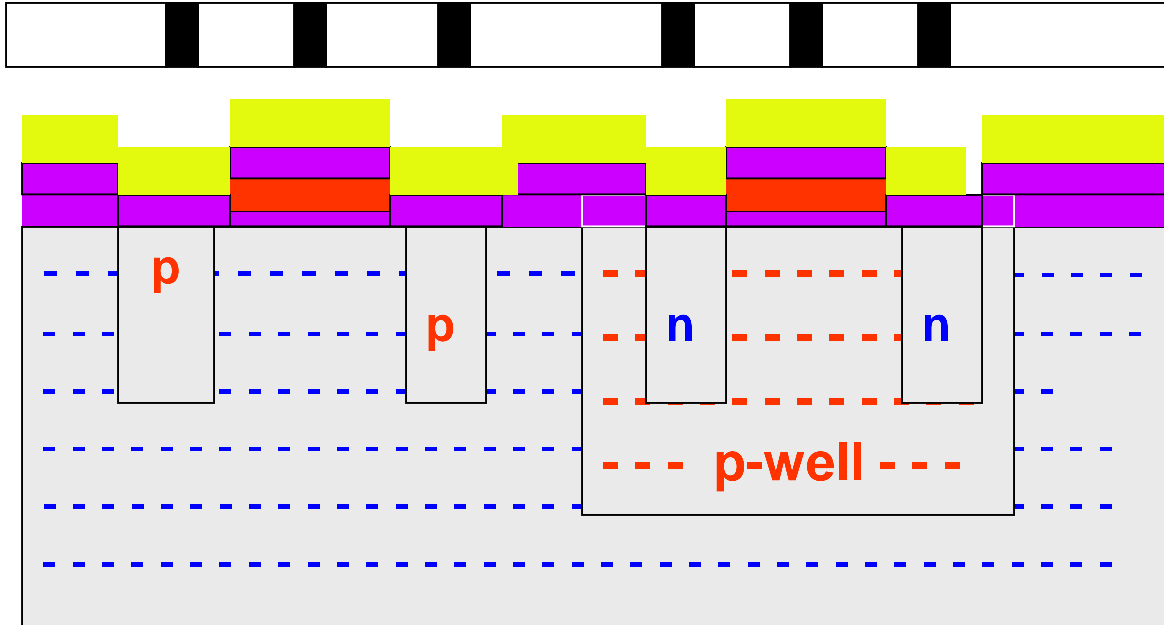


N-MOS Fabrication Process

[[Step- Formation of Contact-Cut]

Mask-6 is used for the formation of Contact – Cuts in S, D and G of n-MOS and p-MOS



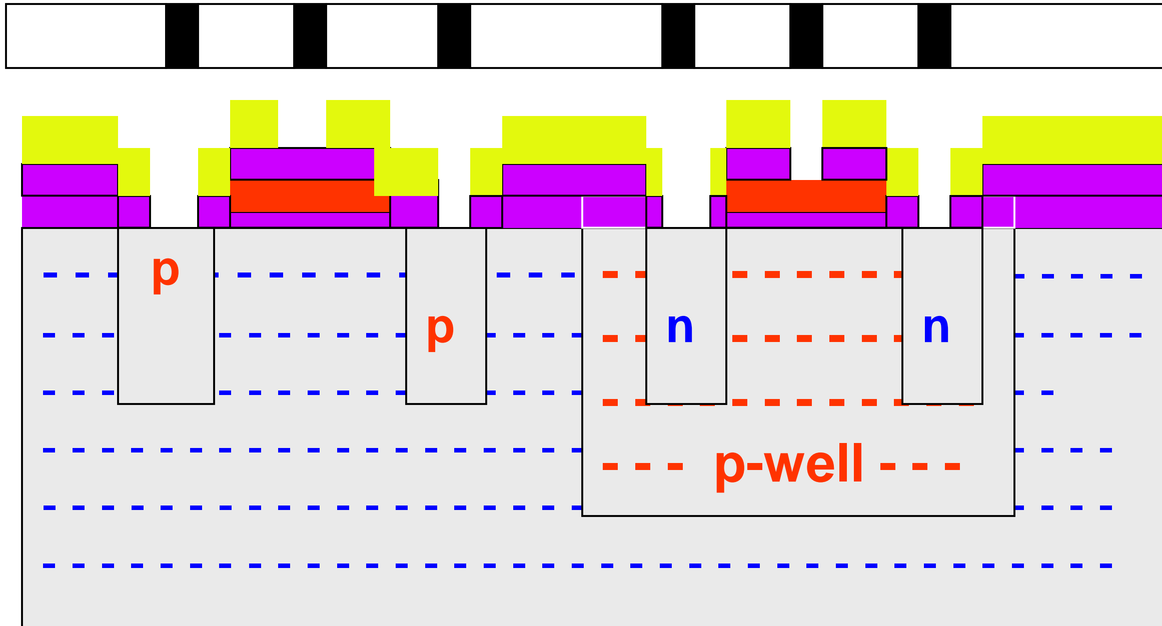


Mask-6

N-MOS Fabrication Process

[[Step- Formation of Contact-Cut]

Mask-6 is used for the formation of Contact – Cuts in S, D and G of n-MOS and p-MOS

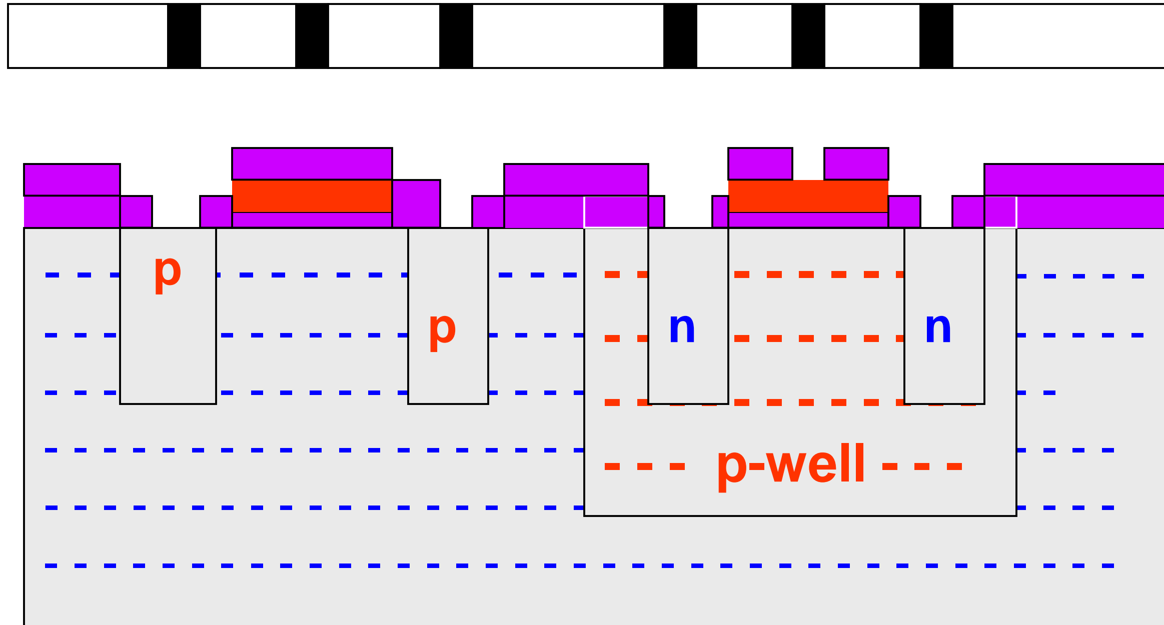


Mask-6

N-MOS Fabrication Process

[[Step- Formation of Contact-Cut]

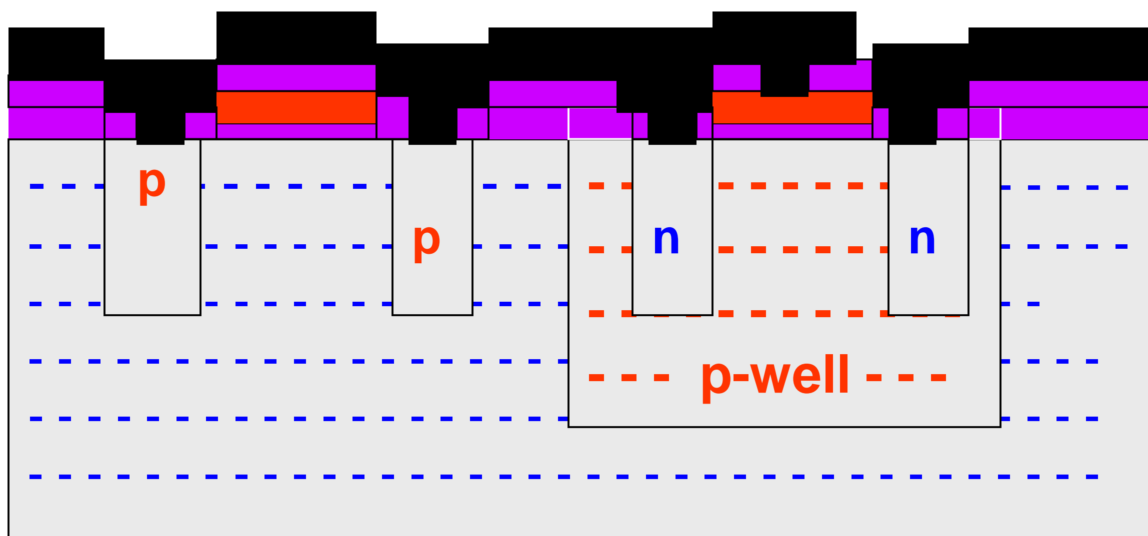
Mask-6 is used for the formation of Contact – Cuts in S, D and G of n-MOS and p-MOS



Mask-6

N-MOS Fabrication Process

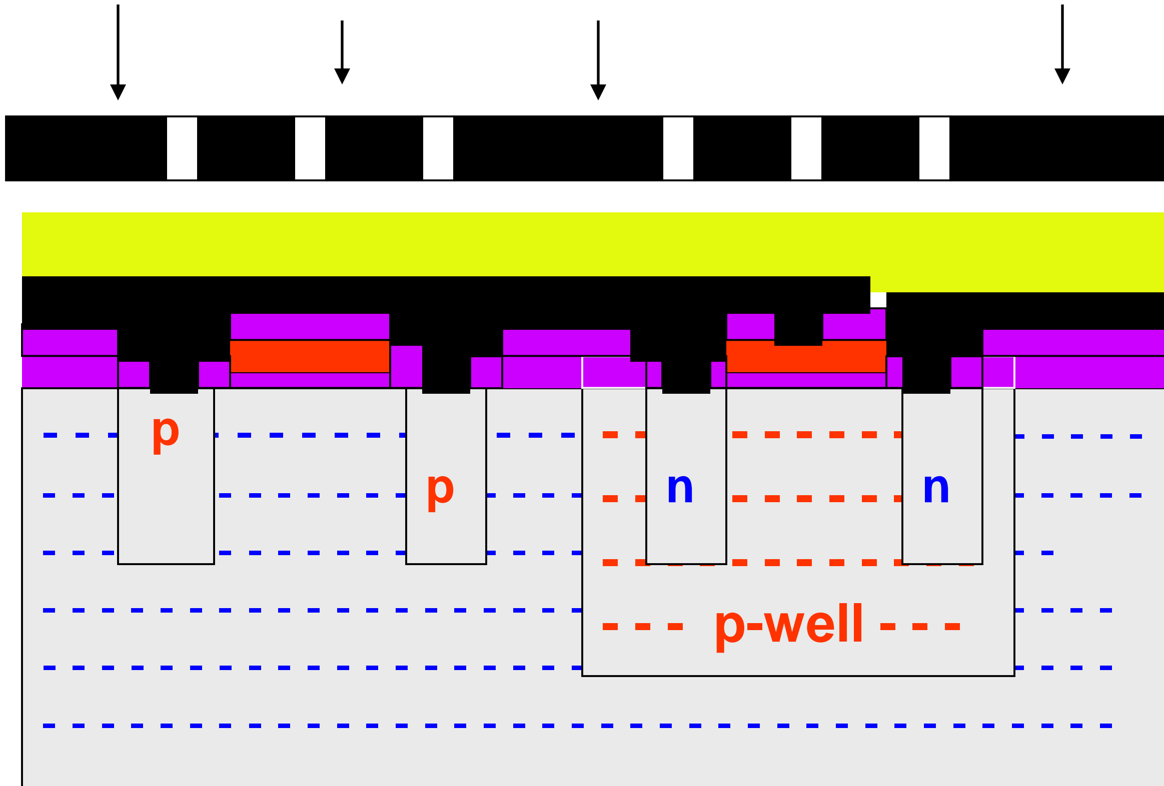
[[Step- Metakkization]



N-MOS Fabrication Process

[[Step- Metakkization]

Mask-7 is used for the deposition of metal in contact - cuts

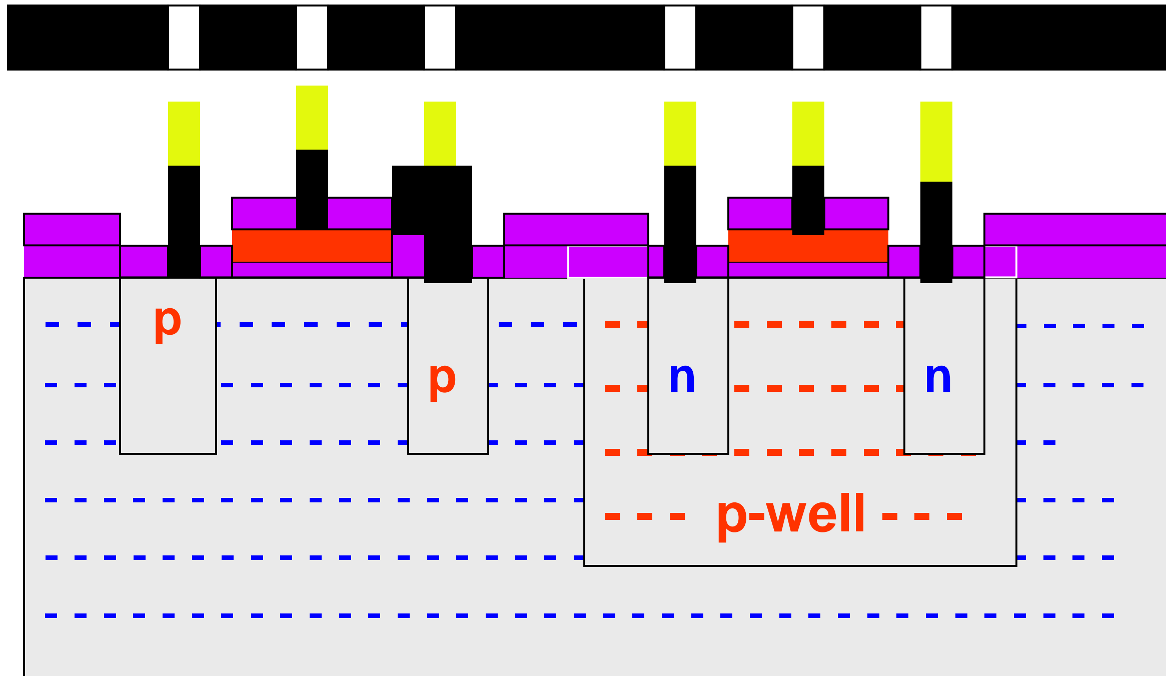


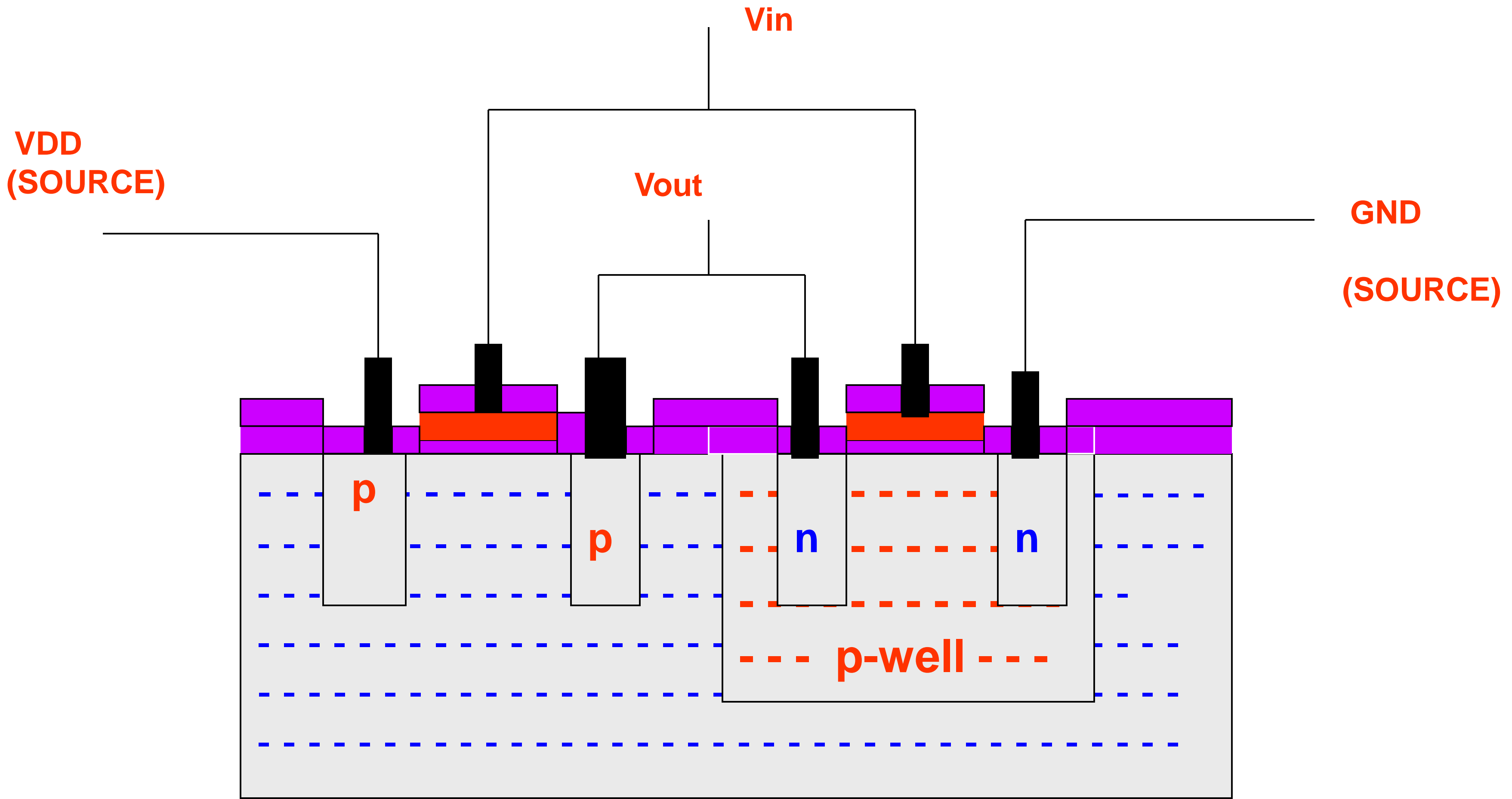
Mask-7

N-MOS Fabrication Process

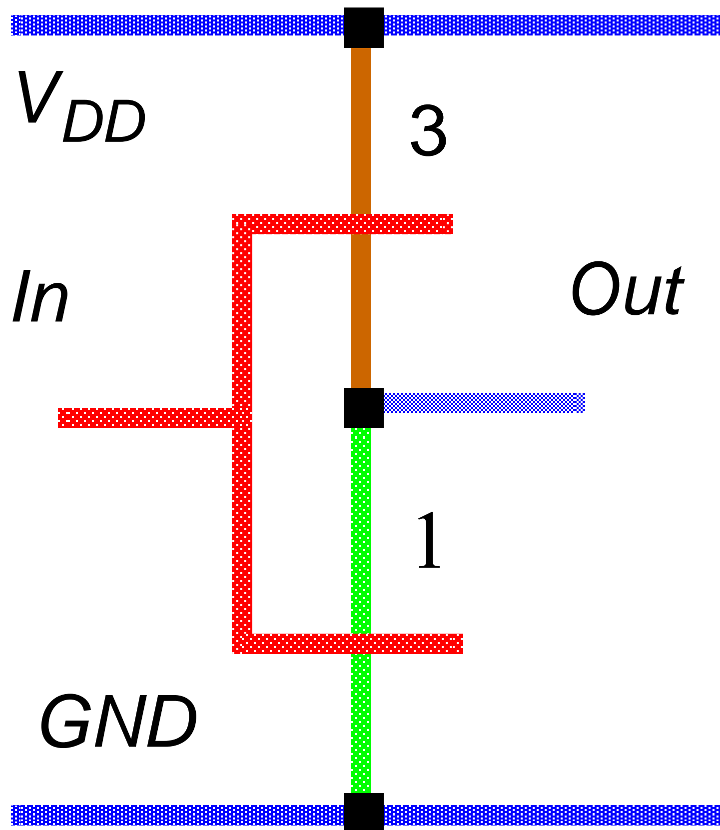
[[Step- Metakkization]

Mask-7 is used for the deposition of metal in contact - cuts




Vin
VDD
(SOURCE)
Vout
GND
(SOURCE)
p
p
n
n
p-well

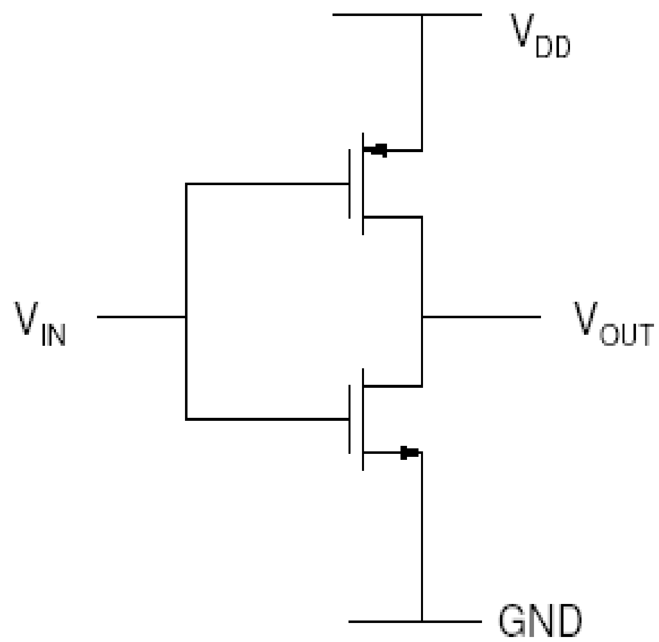
Sticks Diagram

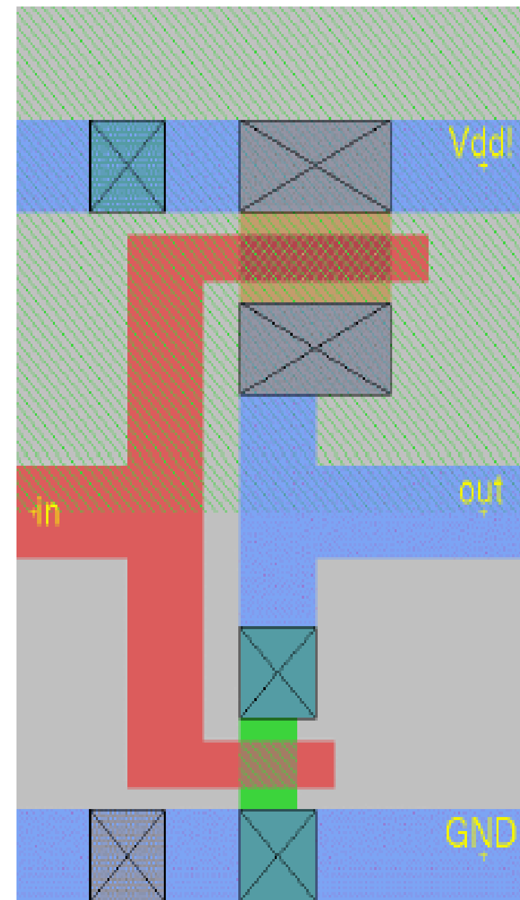


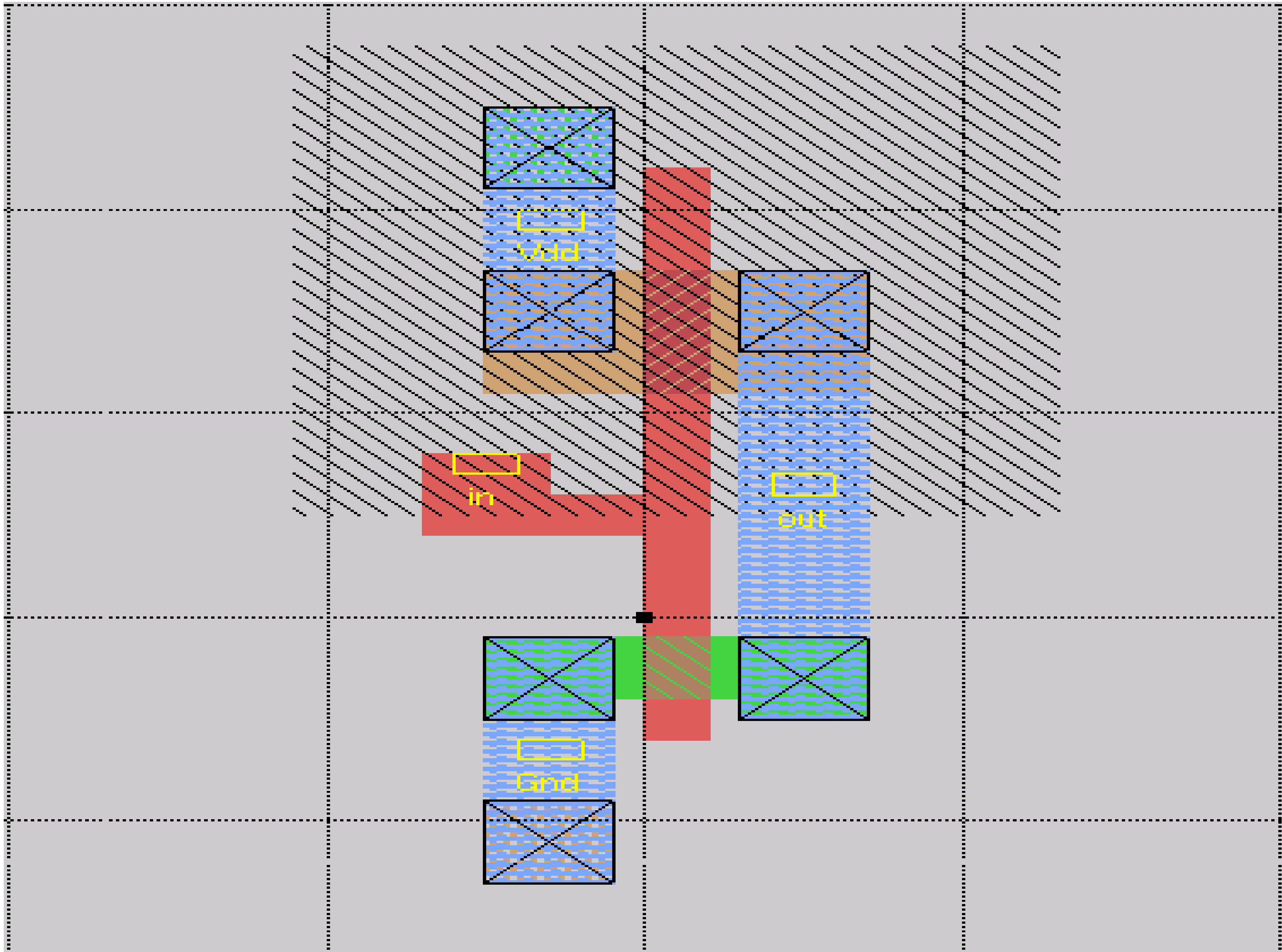
Stick diagram of inverter

- Dimensionless layout entities
- Only topology is important
- Final layout generated by “compaction” program

Layout Design






Vdd
in
out
Gnd